IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Karl M.J. Lofgren et al.		
Title:	Device and Method for Controlling Solid-State Memory System		
Application No.:	10/809,061	Filing Date:	March 24, 2004
Examiner:	Mai, Son Luu	Group Art Unit:	2827
Docket No.:	SNDK.015US7	Conf. No.:	6999

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APPELLANT'S BRIEF UNDER 37 C.F.R. 41.37

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

In response to the Notification of Non-Compliant Appeal Brief mailed on October 11, 2006, and Pursuant to 37 C.F.R. § 1.191 and the Notice of Appeal filed in this application on May 3, 2006, Applicants submit this revised Appeal Brief. The Summary of Claimed Subject Matter section has amended to conform to the remarks of the Notification. The Commissioner is authorized to deduct any amounts required for this Appeal Brief and to credit any amounts overpaid to Deposit Account No. 502664.

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I. REAL PARTY IN INTEREST

The real parties in interest are SanDisk Corporation, a corporation of the state of Delaware, and Western Digital Corporation, a corporation of the state of Delaware, the assignees of all rights, titles and interests in the present patent application from the inventors, Karl M. J. Lofgren, Robert D. Norman, Jeffrey Donald Stai, Anil Gupta and Sanjay Mehrotra.

II. RELATED APPEALS AND INTERFERENCES

A Notice of Appeal was filed on April 26, 2006, for US patent application number 10/785,373, of which the present application is a continuation.

III. STATUS OF THE CLAIMS

The subject application was filed March 24, 2004, and is a continuation of Application No. 10/785,373, filed February 23, 2004, and is in turn a continuation of Application No. 09/939,290, filed on August 22, 2001, which is a continuation of Application No. 09/657,369, filed on September 8, 2000, now Patent No. 6,317,812, which in turn is a continuation of Application No. 09/064,528, filed on April 21, 1998, now Patent No. 6,148,363, which in turn is a continuation of Application No. 08/931,193, filed on September 16, 1997, now Patent No. 5,806,070, which in turn is a continuation of Application No. 08/396,488, filed on March 2, 1995, now abandoned, which in turn is a divisional of Application No. 07/736,733, filed on July 26, 1991, now Patent No. 5,430,859. The original parent application claims 1-39 were cancelled in a Preliminary Amendment filed concurrently with the subject application on March 24, 2004. This Preliminary Amendment also added claims 40-57, which were respectively copies of claims 1-18 of U.S. patent number 6,538,926, of Kato *et al.* issued March 25, 2003.

An Office Communication mailed on August 17, 2004, was a 30-day, non-extendable requirement for information under 37 CFR 1.607 based upon the pending claims, to which a response, cancelling claims 41-46 and 52, was filed on September 16, 2004. An Office Action mailed on April 15, 2005, rejected remaining claims 40, 47-51, and 53-57 under the written description requirement of 35 U.S.C. §112, first paragraph, to which a reply was filed on September 14, 2005. The reply of September 14, 2005, amended claims 40, 51, and 53. An

Office Action mailed on December 9, 2005, again rejected the pending claims under the written description requirement of 35 U.S.C. §112, first paragraph, and made the rejection final.

Claims 1-39, 41-46 and 52 have been cancelled and claims 40, 47-51, and 53-57 are unchanged since the Amendment of September 14, 2005. Claims 40, 47-51, and 53-57 stand rejected under 35 U.S.C. §112, first paragraph, as the Applicants allegedly failed to comply with the written description requirement with respect to the element of a "buffer memory [having] a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation".

IV. STATUS OF AMENDMENTS

On May 3, 2006, a Notice of Appeal from the Examiner's decision rejecting claims 40, 47-51, and 53-57 was filed. No Amendments have been filed since the December 9, 2005, mailing date of the Office Action from which this Appeal is being taken.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As background, this section gives a summary of the present invention. Since the claims stand rejected under the written description requirement of 35 U.S.C. §112, first paragraph, some of this material is presented in more detail below in section VII in order to demonstrate that the specification of the subject application fulfils the written description requirement.

The claimed subject matter relates to a non-volatile memory system having one or more non-volatile memories, each having plurality of cells, and having a buffer memory, and a controller that can receive data from outside of the system and send it to the non-volatile memories to be programmed. When programming, the memory stores data received from the controller in the buffer memory, and from the buffer memory to the memory cells. While the memory is programming, the controller can receive data from outside of the system. The buffer memory has a capacity allowing it to transfer a unit of data equal to the unit in which data is programmed, where this unit is greater than one byte.

The pending independent claims are claims 40 and 51. In claim 40, the memory system is presented as having "a non-volatile memory":

40. A nonvolatile memory system comprising:

a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and

a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,

wherein said nonvolatile memory is enabled to operate a program operation,

wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and

wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claim 51 differs in having "a plurality of non-volatile memories":

51. A nonvolatile memory system comprising:

a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a buffer memory; and

a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,

wherein said nonvolatile memories are enabled to operate a program operation,

wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said buffer memory thereof and stores said data in said buffer memory to ones of said nonvolatile memory cells of that nonvolatile memory,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and

wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

The present application shows such memory systems generally in Figures 1A, 1B, 2A, 2B, and 3. These figures show a memory system 129 having a control module 133 and a number of non-volatile memory devices 141, where the exemplary embodiment organizes the memories into modules 131, 132. These figures and the general arrangement of the system are described in paragraphs [0042]-[0055]. (References are to the clean version of the Substitute Specification that was included when the present application was filed.) A particular memory device 141 is shown in Figure 4, whose description begins with paragraph [0056], with details shown in

Figures 5 and 6, whose descriptions begin at paragraph [0067]. The controller 133 is presented in more detail in Figures 7 and 8, whose description begins with paragraph [0082].

As shown in Figure 1, the controller module is coupled to the memory devices to receive data from outside of the system on 123/138 and then apply it to the memory modules on 135. As shown in Figure 4, data is received at serial protocol logic 203, from which it is transferred along WRITE Data Bus 347 to the WRITE Circuit 211, which in turn programs the data into the array of nonvolatile memory cells 201. An embodiment of the Serial Protocol Logic is shown in more detail in Figure 6A and described beginning at paragraph [0072]. As described in paragraph [0075], incoming data is loaded into element 337, where it is held until it is output onto the WRITE data bus 347.

A write process as seen from the controller side is described beginning at paragraph [0105]. The discussion of transferring data from the controller to a memory device is given in paragraphs [0106]-[0108]. A "chunk" (the unit of data write, see, e.g., line 1 of paragraph [0093]) of data is transferred into the device, after which the programming sequence begins.

The reception of the data on the memory device, where it is stored into element 337 and interpreted as data, is described in paragraph [0081]. The last part of paragraph [0075] describes how the register 337 then outputs a chunk (the unit of data programmed at one time) onto Write data bus 347 for the write circuitry 211.

The ability of the controller to continue to receive data from outside while the program operation is occurring is described in paragraph [0107].

The last part of paragraph [0075] notes that the register 337 is able to transmit a chunk (the unit of data programmed at one time) as it "outputs it [a chunk of data] in parallel on" the Write data bus 347.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Board is asked to review the correctness of the rejections under 35 U.S.C. §112, first paragraph. Specifically, claims 40, 47-51, and 53-57 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written requirement with respect to the "wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to

the data length of said data to be stored at one time of said program operation" element of the claims.

More specifically, the Office Action states:

> There is no support in the specification for the claim limitations "wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation," (claim 40, lines 12-14 and claim51, lines 13-51) in the application as filed.

Claims 47-50 and 53-57 are rejected as they respectively depend on claims 40 and 51. This is the basis for rejecting all of the claims and is the sole issues in this appeal.

All of the claims stand rejected under the same grounds and can be taken to form a single group, with independent claim 40 suitable for deciding whether this group of claims patentable.

VII. ARGUMENT

The most recent Office Action, from which this Appeal originates, rejects all of the pending claims under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement for the "wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation" limitation, as described in the preceding section. All of the claims are rejected on the same grounds, with all of the claims being argued together. When reference to a specific claim is required, claim 40 is believed suitable for this purpose. As described below, it is believed that the written description requirement is fully met.

More specifically, referring to claim 40, the relevant element reads:

> wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation ... .

The antecedent for "said buffer memory" in claim 40 is

> a nonvolatile memory including ... *a buffer memory*..., wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to *said buffer memory* and stores said data in *said buffer memory* to ones of said nonvolatile memory cells,

where the emphasis is added to make the occurrences the occurrences of this element easier to see. The buffer memory of the claims corresponds to the register 337 of Figure 6A. More explicitly, as described in paragraphs [0072]-[0075], the memory device 141 (Figures 2, 3, 4) receives data from the controller 133 or 134 in serial form on lines SI0 237 and SI1 239 where it is received in the serial protocol logic 205 (Figure 4). As shown in the detail of the serial protocol logic 205 of Figure 6A, the serial data on SI0 and SI1 is accumulated register 237. Once a "chunk" is accumulated in the register 237, it can be output onto the WRITE data 347 and (returning to Figure 4) written by the write circuitry 211 into the nonvolatile memory 201. In the present application, the unit in which data is programmed (and also read) is the "chunk", which the exemplary embodiment takes as having a size of 64 bits. This is noted in noted, for example, in the first line of paragraph [0093]: "In the preferred embodiment, data is written and read in 64-bit chunks."

Consequently, the relevant element of claim 40 is equivalent to the register 337 having a data storing capacity enabling the transfer of a chunk of data. This is described in the last sentence of paragraph [0075]:

> Similarly, the *data shift register* 337 shifts in a 64-bit chunk of data, and ***outputs it in parallel*** on a WRITE data bus 347.

As the added emphasis shows, register 337, that corresponds to the buffer memory, has a capacity allowing it to transmit a chunk of data, which is "a unit of data of a length equal to the data length of said data to be stored at one time of said program operation". Consequently, it is believed that the present application meets the written description requirement with respect to the "wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation" element of the claims.

In its rejection, the Office Action states that "The shift register 337 does not have a data storing capacity enabling the receiving of a unit of data length equal to the data length of the data to be stored at one time of the program operation as claimed in claims 40 and 51." First, it should be noted that claims correctly read "data storing capacity enabling the *transfer*", rather than receiving, "of a unit of data ...", where the emphasis is added. In any case, it is respectfully submitted that this statement of the Office Action is directly contradicted by the specification of the present application: as stated in last sentence of paragraph [0075] that is quoted above, register 337 is able to

output a chunk of data in parallel. Thus, it has the capacity to store a chunk of data, which is "a unit of data length equal to the data length of the data to be stored at one time of the program operation".

The Office Action also makes the statement that "A shift register 337 in figure 6A of the instant application is a data shift register, which function is to shift data from its input to output." There relevance of this statement is unclear: the claim states that the "buffer memory" of the claims "stores said data [received "from said control device"]" and "stores said data ... to ones of said nonvolatile memory cells"; that is, it receives data at its input (from the controller) and then outputs it (as it is programmed into the array), which is what the Office Action appears to find objectionable about register 337. Although unclear from its remarks, the Office Action's objections may be based on assuming that element 337 shifts each bit of data out as it is received; however, this is also contradicted by noting that register 337 outputs a 64-bit chunk of data in parallel and, consequently, must accumulate the data shifted in serially until it contains the whole chunk.

(Although not explicitly stated, it may be that the Office Action is rejecting the use of the words "buffer" in the claims, while element 337 in Figure 6A is labeled as a "register". The specification does not call element 337 by the name of a "buffer", instead using "register"; however, this is a much more stringent requirement than is needed to satisfy the written description requirement of 35 U.S.C. §112, first paragraph, and would be an improper basis for a rejection. As discussed in detail in the M.P.E.P. at §2111, and specifically in §2111.01, "The words of a claim must be given their 'plain meaning' unless they are defied in the specification". There is nothing in specification that defines "buffer" to have anything other than its plain meaning, namely an element for the temporary storage of data, which the specification clearly describes register 337 as being. As discussed above, the specification describes that data shift register 337 temporally stores the data content to be written in a programming operation.

This point is considered in the third paragraph of section 2163.02 of the M.P.E.P.. This states (where the emphasis has been added) that:

> The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.

The "Burden on the Examiner with Regard to the Written Description Requirement" is the subject of section 2163.04 of the M.P.E.P.. This states (where the emphasis has been added) that:

> ... A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. ... The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. *The examiner has the initial burden of presenting* ***by a preponderance of evidence*** *why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims.*

It is respectfully submitted that, if the use of "buffer" rather "register" is the basis of the rejection, not only has the Examiner failed to make this explicit in the Office Action, but has also failed to present "a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims".

Alternately, or perhaps additionally, it could be that the Office Action is reading limitations into the claim that are not actually found in the claim: As noted above in Section III above, the currently pending claims in the present application are based on claims from U.S. patent number 6,538,926, of Kato *et al.*. The Office Action may be reading limitations of a specific embodiment of this patent into the claim and then requiring the present application to support this particular embodiment. This is improper. The correct question is whether the present specification is enabling for the claims ***as written***. (Although not explicitly made in the Office Action here, this error was explicitly made in the parent to the present application, which, as noted above in Section II, is currently under appeal based on such an improper rejection.))

VIII. CONCLUSION

It is Applicants' position, as indicated above, that the assertions of the Office Action are incorrect. As described above, it is believed that the disclosure provided by the subject application fully meets the written description requirement. Accordingly, the rejection of the application should be reversed and the present patent application found allowable.

Respectfully submitted,

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Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 10/809,061

(Claims 1-39 have been cancelled.)

40. A nonvolatile memory system comprising:

a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and

a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,

wherein said nonvolatile memory is enabled to operate a program operation,

wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and

wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

(Claims 41-46 have been cancelled.)

47. A nonvolatile memory system according to claim 40,

wherein said nonvolatile memory includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to the corresponding word line and corresponding data line.

48. A nonvolatile memory system according to claim 47,

wherein said nonvolatile memory includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data storing capacity and enabling the storing of a unit of data in said sector.

49. A nonvolatile memory system according to claim 48, wherein said nonvolatile memory is a flash memory.

50. A nonvolatile memory system according to claim 40,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memory and an external system bus.

51. A nonvolatile memory system comprising:

a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a buffer memory; and

a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,

wherein said nonvolatile memories are enabled to operate a program operation,

wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said buffer memory thereof and stores said data in said buffer memory to ones of said nonvolatile memory cells of that nonvolatile memory,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and

wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

(Claim 52 has been cancelled.)

53. A nonvolatile memory system according to claim 51,

wherein each of said nonvolatile memories further includes a plurality of word lines and a plurality of data lines, and

wherein each of said nonvolatile memory cells in each of the nonvolatile memories is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to said corresponding word line and corresponding data line.

54. A nonvolatile memory system according to claim 53,

wherein each of said nonvolatile memories includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and

wherein said buffer memory has a data storing capacity for receiving data in units of a sector and enabling the storing of a unit of data in said sector.

55. A nonvolatile memory system accordance to claim 54,

wherein each of said nonvolatile memories is a flash memory.

56. A nonvolatile memory system according to claim 55,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.

57. A nonvolatile memory system according to claim 51,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the. nonvolatile memories and an external system bus.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.